

## **High Gain DC/DC Converter for Photovoltaic Applications**

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## ABSTRACT

As far renewable energy is concerned solar photovoltaic means of energy production plays a major role. Since sun's energy is available in abundant not completely its source is utilized by the photovoltaic cells. So, efficiency of the energy conversion scheme should be high. Hence a high-efficiency dc–dc converter is proposed for low-voltage photovoltaic sources. The proposed converter boosts up the DC voltage with high voltage gain and high efficiency. The proposed converter uses dual active clamping circuit and resonant voltage doubler rectifier. At low voltage side, the voltage stress of power switches is reduced. At high-voltage side, zero-current turn-off of output diodes is achieved.

*Keywords*-DC-DC converter; photovoltaic(PV); power efficiency.

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### I. INTRODUCTION

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The photovoltaic (PV) module-integrated converter (MIC) system is the key technology for future production of electricity using solar energy [4], [5]. Each PV module has its own power conversion system. The power conversion system generates the maximum power from the PV module [7]. To make the PV MIC system commercially viable, a highefficiency and low- cost power conversion scheme should be developed. Generally, the PV module has a low-voltage characteristic [15]. In order to deliver electric power into the grid, the low voltage (dc voltage of PV module) should be converted into high dc voltage [14]. Therefore, a high-voltage gain dc-dc converter is needed.

The switch voltage stress of the integrated cascade boost converter is equal to high voltage, and the current stress is large [1]. Cascade boost converter increases the conduction losses and reduces the efficiency of the converter. A converter with a coupled inductor can easily improve the voltage gain by increasing the turns ratio of the coupled inductor. However, it has a large steady- state inductance. The large steady state inductance increases losses and hence reduces the overall efficiency [12]. Additionally, the converter layout is complex and the design procedure is also relatively complex. The SC converters will not require the magnetic components, such as the inductor or the transformer. Thus the switching frequency can be increased to a high level. However, a large number of power devices are required to achieve high-voltage-gain, which increases the complexity and cost of the converter [6].

Most of the single-phase isolated DC/DC converters seem insufficient and deficient as their components are not able to handle the high power conditions. In the Multiphase Dual Active Bridge Converter, the losses of the converter increase, as the phase shift increases. Additionally, the topology involves two switch legs which require 12 power switches for a three-phase converter and thus it increases the number of switches, thereby the switching losses and the converter cost [10].The Multiphase ZVS PWM DC/DC Converter suffers from limited duty cycle owing to large leakage inductance (0 < D < 0.333), and experiences high circulating energy in the primary side during the free-wheeling periods [3].

The active-bridge dc–dc converter has been used for photovoltaic sources [9], [2]. The power switches at low-voltage side are turned on at zero voltage. However, the output diode at high-voltage side has high switching power losses because of its reverserecovery current. The half-bridge dc–dc converter has been presented to reduce the switching power losses at high voltage side [16]. The output diodes are turned off at zero current by voltage doubler rectifier circuit. However, an additional half-wave rectifier is needed here, which increases the switching power losses. Alternatively, the active-clamped dc–dc converter has been used for low-voltage PV sources [8], [13]. It uses the active-clamping circuit and the resonant voltage doubler rectifier circuits.

This paper proposes a high-efficiency dc–dc converter for low- voltage PV sources. An activeclamped dc–dc converter is presented by using a dual active-clamping circuit. The voltage stress of power switches are reduced at low-voltage side. The



operation of the proposed converter is explained. The performance of the proposed converter is verified using the PSIM software. The simulation results show that a high efficiency of 98% is achieved at 41-V input voltage for 330-W output power.

### II. PROPOSED DC-DC CONVERTER

#### A. Converter Description

The proposed DC/DC converter with dual active clamping circuit and voltage doubler rectifier is shown

in fig. 1. The proposed DC/DC converter is of AC link chopper type. The inverter portion is made with dual active clamping circuit. Resonant voltage doubler rectifier is used in the rectifier portion. The proposed DC/DC converter has main switches ( $S_1$ ,  $S_4$ ), the dual active-clamping circuit ( $S_2$ ,  $S_3$ ,  $C_c$ ), transformer T, and resonant voltage doubler rectifier ( $L_{lk}$ ,  $C_r$ ,  $D_{o1}$ ,  $D_{o2}$ ). The main switches ( $S_1$ ,  $S_4$ ) and auxiliary switches -

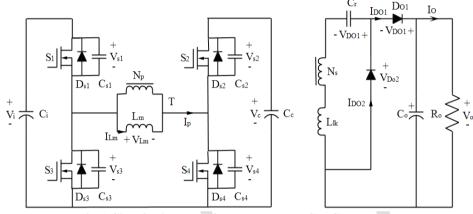


Fig.1 Circuit diagram of the proposed DC-DC converter

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 $(S_2,\,S_3$ ) are made to operate complementarily with a short dead time. All the switches are metal–oxide–semiconductor -field-effect transistors. They are considered as ideal switches except their output capacitors  $C_{S1}$ – $C_{S4}$  and body diodes  $D_{S1}$ – $D_{S4}$ .  $C_i$  is the input capacitor.  $C_c$  is the clamping capacitor.  $C_o$  is the output capacitor. The capacitors  $C_i,\,C_c$  and  $C_o$  are very large enough so that their voltages  $V_i,\,V_c,\,$  and  $V_o$  are considered constant, respectively. The transformer has the magnetizing inductor  $L_m$  and leakage inductor  $L_{lk}$ .  $L_{lk}$  is assumed to be much smaller than  $L_m$ . The turns ratio of the transformer is 1:N, where  $N=N_s/N_p$ . The capacitor  $C_r$  is the resonant capacitor.

### B. Converter Operation

Fig. 2 shows the switching waveforms of the proposed DC-DC converter during one switching period  $T_s$  (=1/f<sub>s</sub>). The switching waveforms at the primary side are shown in fig. 2(a). Fig. 2(b) shows the switching waveforms at the secondary side. The proposed DC/DC converter has six switching modes during  $T_s$ . The duty ratio D is based on the on-time of main switches. Before t = t<sub>0</sub>, S<sub>2</sub> and S<sub>3</sub> have been turned OFF. The voltages V<sub>S1</sub> and V<sub>S4</sub> have been zero when the primary current i<sub>p</sub> flows through the body diodes D<sub>S1</sub> and D<sub>S4</sub>.

1) Mode  $l[t_0, t_1]$ : At t = t<sub>0</sub>, S<sub>1</sub> and S<sub>4</sub> are turned on. The current through the inductor is given by the equation

$$i_{Lm} = V_{L_m}/L_m$$
(1)
$$i_{Lm} = V_{i, the current} i_{Lm} is given by$$

$$i_{Lm} = V_i/L_m$$
(2)

So, the magnetizing inductor current  $i_{Lm}$  increases linearly as

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{V_i}{L_m}(t - t_0)$$
(3)

At the secondary side,  $NV_i$  is applied to the secondary winding of T. The output diode  $D_{\rm o1}$  is turned on. The series- resonant circuit is formed which consists of  $C_r$  and  $L_{\rm lk}$ . By this series resonance between  $L_{\rm lk}$  and  $C_r$ , the energy stored in  $C_r$  is transferred to the output capacitor  $C_o$ . The angular resonant frequency  $\omega_r$  of the series-resonant circuit is

$$\omega_{\rm r} = 2\pi f_{\rm r} = 1/\sqrt{L_{\rm lk}C_{\rm r}}$$
(4)

Where  $f_r$  is the resonant frequency.

By referring the output diode current  $i_{\text{Dol}}$  to the primary

side, the primary current  $i_p$  can be expressed as  $i_i(t) = i_i(t_i) + \frac{V_i}{V_i}(t_i - t_i) + N_i$ 

$$i_p(t) = i_p(t_0) + \frac{v_1}{L_m} (t - t_0) + Ni_{DO1}(t)$$
(5)

The resonant impedance  $Z_r$  can be expressed as  $Z_r = \sqrt{L_{lk}/C_r}$ 

$$Z_{\rm r} = \sqrt{L_{\rm lk}/C_{\rm r}}$$
(6)



2) Mode  $2[t_1, t_2]$ : At  $t = t_1$ , the half-resonant period of the series resonance is finished. The current through the output diode  $iD_{o1}$  is zero before  $D_{o1}$  is turned OFF. Thus the output diode,  $D_{o1}$  is turned off at zero current without any diode reverse recovery current.

3) Mode 3 [ $t_2$ ,  $t_3$ ]: The primary current  $i_p$  charges  $C_{S1}$ , $C_{S4}$  and discharges  $C_{S2}$ , $C_{S3}$ .  $V_{S1}$  and  $V_{S4}$  increase from zero to  $V_i$ .  $V_{S2}$  and  $V_{S3}$  decrease from  $V_c$  to zero. Since the switch output capacitor  $C_S$  (=  $C_{S1}$ =  $C_{S2}$ =  $C_{S3}$ = $C_{S4}$ ) is very small, the time interval during this mode is considered negligible compared to  $T_s$ .

4) Mode 4 [ $t_3$ ,  $t_4$ ]: At t = t<sub>3</sub>, S<sub>2</sub> and S<sub>3</sub> are turned ON. Since V<sub>Lm</sub> = -V<sub>c</sub>, i<sub>Lm</sub> is given by

$$i_{\rm Lm} = -V_{\rm c}/L_{\rm m}$$

Therefore, the magnetizing inductor current  $i_{Lm}$  decreases linearly as

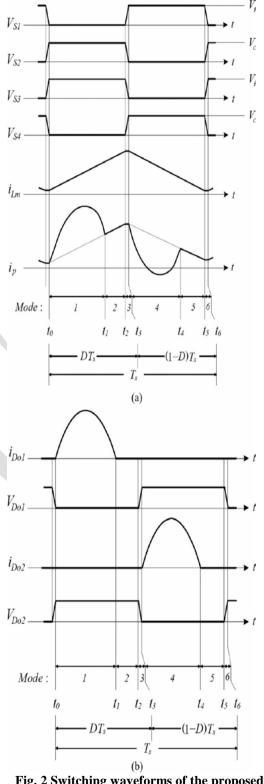
$$i_{Lm}(t) = i_{Lm}(t_3) - \frac{V_c}{L_m}(t - t_3)$$
(8)

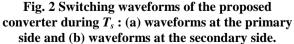
By referring the output diode current  $i_{\text{Dol}}$  to the primary side, the primary current  $i_{\text{p}}$  can be expressed as

$$i_p(t) = i_p(t_3) - \frac{V_c}{L_m} (t - t_3) - Ni_{DO2}(t)$$
(9)

5) Mode 5  $[t_4, t_5]$ : At t = t<sub>4</sub>, the half-resonant period of the series resonance is finished. The output diode current  $i_{Do2}$  is zero before  $D_{o1}$  is turned OFF.  $D_{o2}$  can be turned off at zero current without any diode reverse recovery current.

6) Mode 6 [ $t_5$ ,  $t_6$ ]: At t = t<sub>5</sub>, S<sub>2</sub> and S<sub>3</sub> are turned OFF. The primary current i<sub>p</sub> charges the capacitors C<sub>S1</sub>, C<sub>S4</sub> and discharges C<sub>S2</sub>, C<sub>S3</sub>. The voltages V<sub>S2</sub> and V<sub>S3</sub> increase from zero to V<sub>c</sub>. The voltages V<sub>S1</sub> and V<sub>S4</sub> decrease from V<sub>i</sub> to zero.





Since the switch output capacitor  $C_S$  (=  $C_{S1}$ =  $C_{S2}$ =  $C_{S3}$ = $C_{S4}$ ) is very small, the time interval during this



mode is considered as negligible compared to  $T_s$ . The next switching cycle begins when  $S_1$  and  $S_4$  are turned ON again.

# *C.* Variation of clamping capacitor voltage with duty cycle

The principle of inductor volt-second balance states that the average value, or dc component, of voltage applied across an ideal inductor winding must be zero. This principle also applies to each winding of a transformer or other multiple winding magnetic devices. By the voltage-second balance relation on the magnetizing inductor  $L_m$ , the voltages  $V_c$  and  $V_r$  are expressed as

$$V_{c} = [D/(1-D)] V_{i}$$
  
(10)  
 $V_{r} = (1-D) V_{o}$   
(11)

For the voltage-second balance relation on the secondary winding of T during  $T_s$ , the following relation between the output voltage  $V_o$  and the input voltage  $V_i$  is obtained.

$$V_o/V_i = N/(1-D)$$

The maximum voltage stress of  $S_1$  and  $S_3$  is limited to the input voltage  $V_i$ . The voltage stress of  $S_2$ and  $S_4$  is limited to the clamping capacitor voltage  $V_c$ . The relation between the clamping capacitor voltage  $V_c$  and the duty ratio D is shown in fig. 4. The dual active-clamping circuit is used in the inverter part of the proposed DC/DC converter. The clamping capacitor voltage in case of the dual active-clamping circuit is always lower than the clamping capacitor voltage in case of the conventional active-clamping circuit. It means that the switch voltage stress of the proposed DC/DC converter is always lower than the switch voltage stress of the previous converter [12] using the conventional active-clamping circuit. Especially, when the duty cycle ratio is below 0.5, the clamping capacitor voltage  $V_c$  can be lower than the input voltage  $V_i$ . It is critically beneficial in low-voltage PV applications where more than 50% of the power losses are lost as switching power losses.

D. Conditions for zero current turn-off

The output diode currents  $i_{Do1}$  and  $i_{Do2}$  should be zero before the output diodes  $D_{o1}$  and  $D_{o2}$  are turned OFF. The half-resonant period of the series resonance during Mode 1 and Mode 4 should be finished before the output diode is turned OFF. The following conditions should be satisfied for zero-current turn-off of the output diodes.

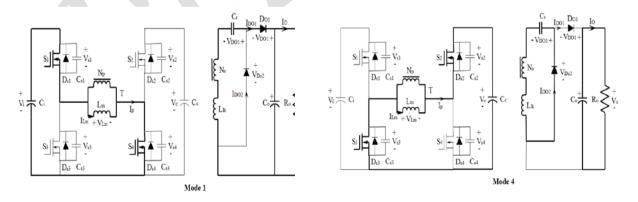
$$\begin{array}{ll} Sin \ [\omega_c D_{max} T_S] \ = 0 & \mbox{if } D_{max} \le 0.5 \\ (13) \\ Sin \ [\omega_c \ (1\text{-}D_{max} \ ) T_S] \ = 0 & \mbox{if } D_{max} > 0.5 \\ (14) \end{array}$$

For zero-current turnoff of the output diode, the resonant frequency,  $f_r$  should be higher than the critical resonant frequency,  $f_c$ . Then, the resonant capacitor  $C_r$  should be determined as

$$C_{\rm r} < \frac{1}{\omega_{\rm c}^2 L_{\rm lk}} = \frac{D_{\rm max}^2 T_{\rm S}^2}{\pi^2 L_{\rm lk}} \quad \text{if } D_{\rm max} \le 0.5$$
$$= \frac{(1 - D_{\rm max})^2 T_{\rm S}^2}{\pi^2 L_{\rm lk}} \quad \text{if } D_{\rm max} > 5$$

# III. SIMULATION RESULTS

To verify the theoretical analysis of the proposed topology, the simulation results are presented using PSIM 9.0 software.



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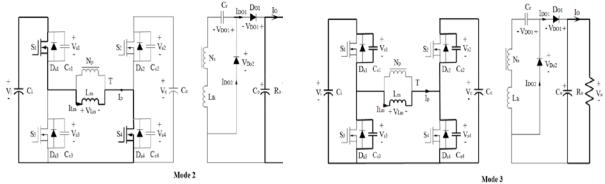


Fig.3 Switching modes of the proposed converter during T<sub>s</sub>

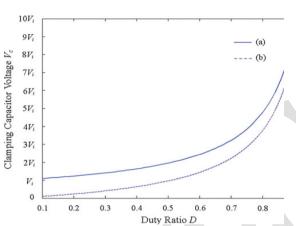
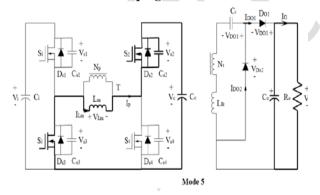
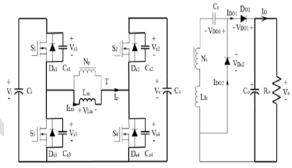


Fig. 4 Relation between the clamping capacitor voltage  $V_c$  and the duty ratio D: (a) in case of the conventional active-clamping circuit and (b) in case of the dual active-clamping circuit.





### **TABLE I** SIMULATION PARAMETERS

Mode 6

Parameters	Value
Input voltage, V <sub>i</sub>	40 V
Output voltage, V <sub>o</sub>	409 V
Output power, Po	330 W
Switching frequency, fs	5 kHz
Input capacitor, C <sub>i</sub>	13.2 nF
Clamping capacitor, C <sub>C</sub>	680 µF
Switch output capacitor, C <sub>S</sub>	500 pF
Transformer turns ratio, N	5
Magnetizing inductor, L <sub>m</sub>	9 µh
Leakage inductor, L <sub>lk</sub>	3 μΗ
Resonant capacitor, C <sub>r</sub>	0.4 µF
Output capacitor, Co	50 µF



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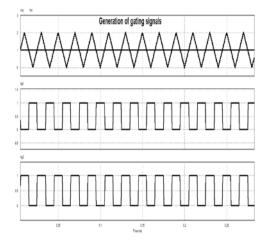


Fig. 5 Waveforms of carrier voltage (V<sub>tri</sub>), DC signal (V<sub>dc</sub>), and gate voltages (V<sub>g1</sub> & V<sub>g2</sub>)

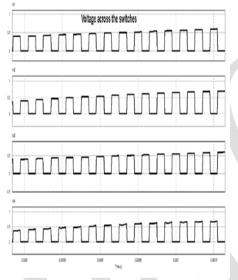


Fig. 6 Waveforms of voltage across switches (V\_{s1}, V\_{s2}, V\_{s3} \ \& \ V\_{s4})

The parameters of various components in the proposed DC/DC converter are given in table I. To apply the gating signals to the gate terminal of the power switches, a triangular and DC signal is compared. By comparing these two signals, we can get equidistant PWM pulses which in turn applied to the gate terminals of the power switches  $S_1$  to  $S_4$ . The voltage across the switches is shown in fig. 6. Fig. 8 shows the simulation waveforms of input and output voltages. The average input voltage is 41 volts. The average output voltage is measured as 409V. Fig. 8 shows the input and output power waveforms. The input power is about 337W. The average output power is measured as 330W. The output power is slightly less than the input power. Thus the proposed DC-DC converter achieves the efficiency of 97.9% and also high voltage gain.

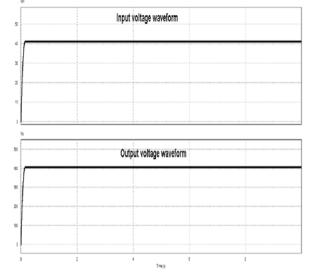


Fig. 7 Input and output voltage (V<sub>in</sub>, V<sub>o</sub>) waveforms

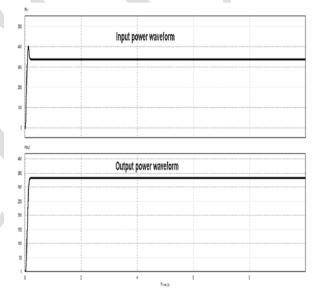


Fig. 8 Input and output power (P<sub>in</sub>, P<sub>o</sub>) waveforms

### IV. EXPERIMENTAL SETUP

The control circuit of the proposed DC/DC converter is shown in Fig.9. In the control circuit, 8051 microcontroller is used with IR2110 driver IC. The power circuit is made with switches  $S_1 = S_2 = S_3 = S_4 = IRFP150$ . The output diodes are of F10A60. To initialize the 8051 microcontroller and to generate the signals, a program is written by using C coding and executed with the help of Keil software. Flash magic software is used to load the program to the microcontroller. The power circuit is triggered by the control circuit which is shown in Fig. 9. The waveforms of gating pulses to the switches  $S_1$ ,  $S_2$  is shown in Fig. 10. The same gating pulse of  $S_1$ ,  $S_2$  can be given to the switches  $S_4$ ,  $S_3$  respectively.



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Fig. 9 Photograph of the designed control circuit

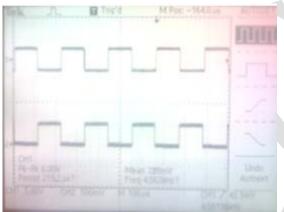


Fig. 10 Waveforms of gating pulses to the switches  $S_1,S_2$ 

### **V. CONCLUSION**

As a solution for providing efficient PV conversion, a high-efficiency and high-gain DC/DC converter has been proposed for low-voltage PV sources. The operation of the

proposed DC/DC converter has been described. The synthesis of the converter was described along with the circuit operating modes and the corresponding key waveforms. The proposed converter reduces the switching power losses, increasing power efficiency. The proposed DC/DC converter topology gives high voltage conversion ratio and zero current turn-off of output diodes.

The proposed DC/DC converter is verified using PSIM. The proposed converter achieves a highefficiency of 98% at 41-V input voltage for 340-Watts output power. Further efficiency improvements are possible with the addition of modified PI controller for output voltage control. By this, the dynamic and transient response can also be improved. In future, the prototype of the proposed DC/DC converter can be made with high gain and high efficiency.

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